OIPE JC182
APR 0 2 2001
PATENT & TRADEMARK OFFICE

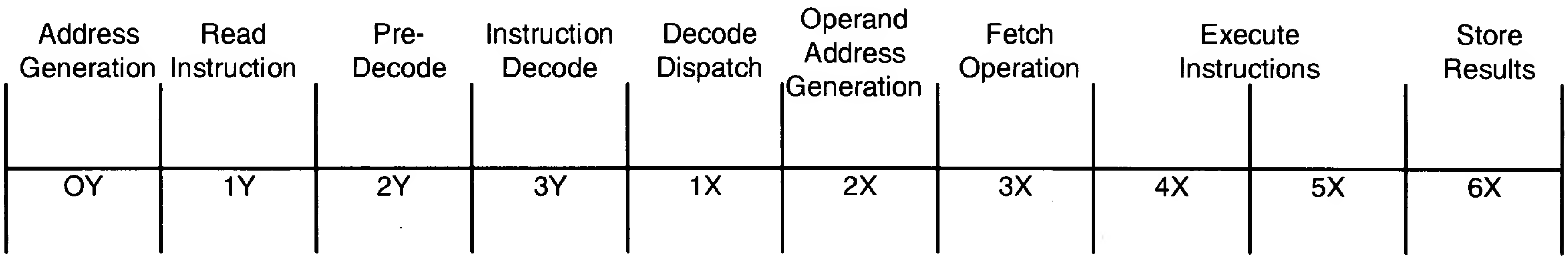

FIG. 1

OIPE JC182
APR 0 2 2001
PATENT & TRADEMARK OFFICE

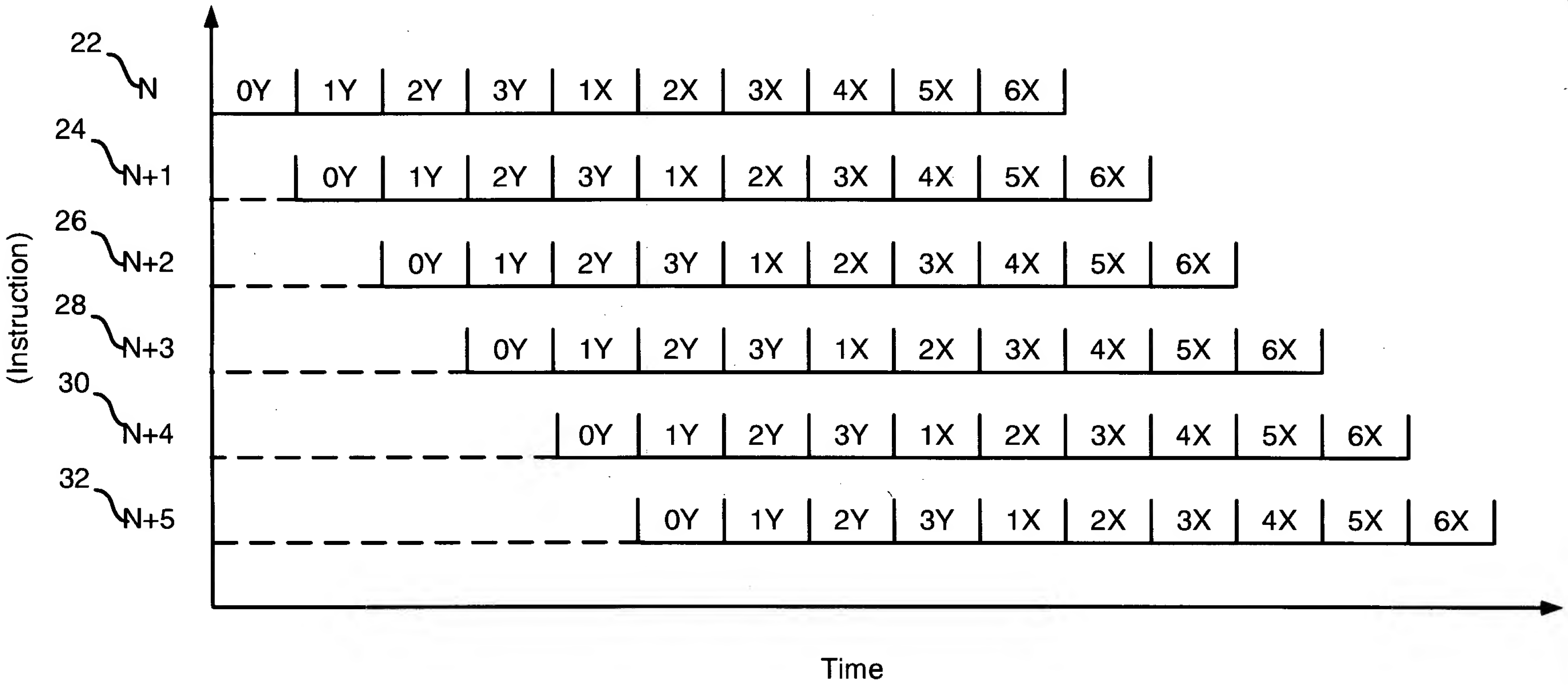

FIG. 2

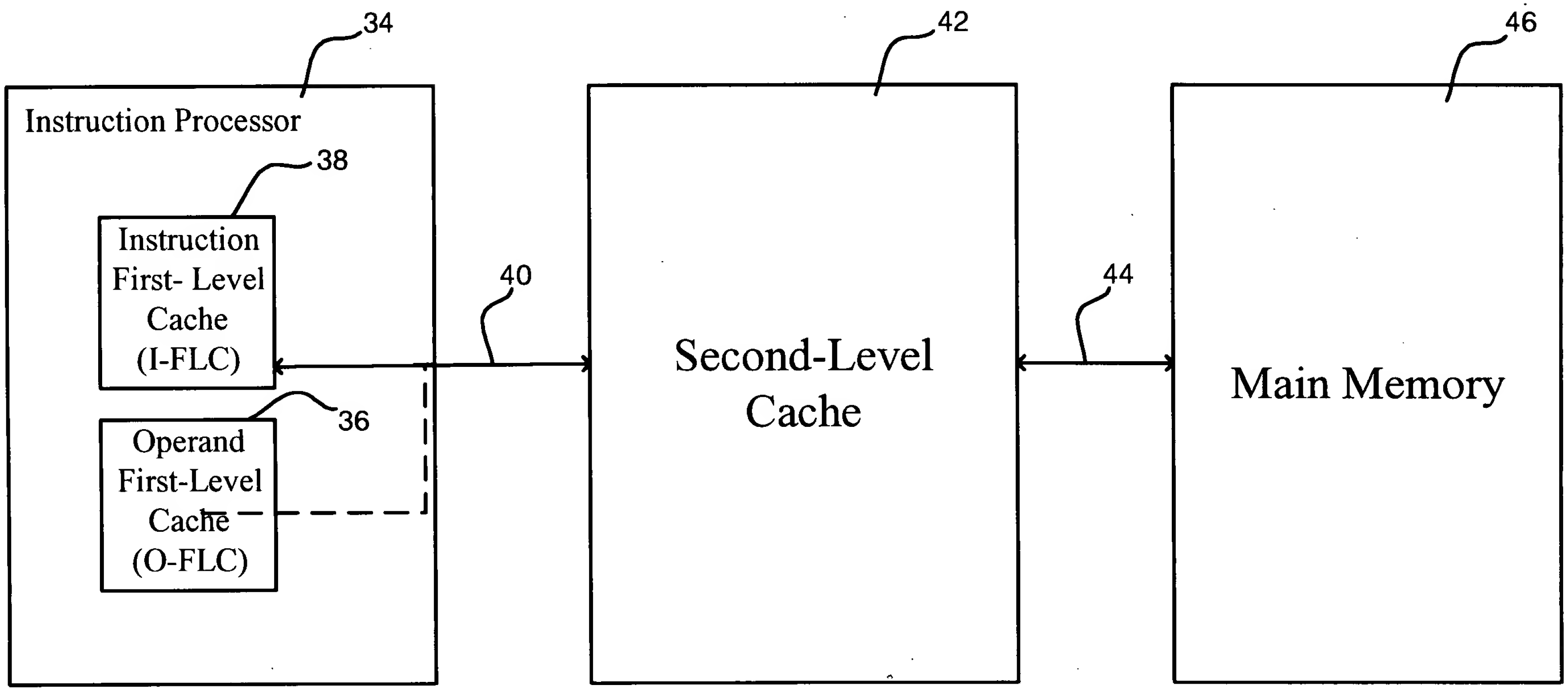
34
Instruction Processor
38
Instruction First- Level Cache (I-FLC)
36
Operand First-Level Cache (O-FLC)
40
42
Second-Level Cache
44
46
Main Memory

FIG. 3

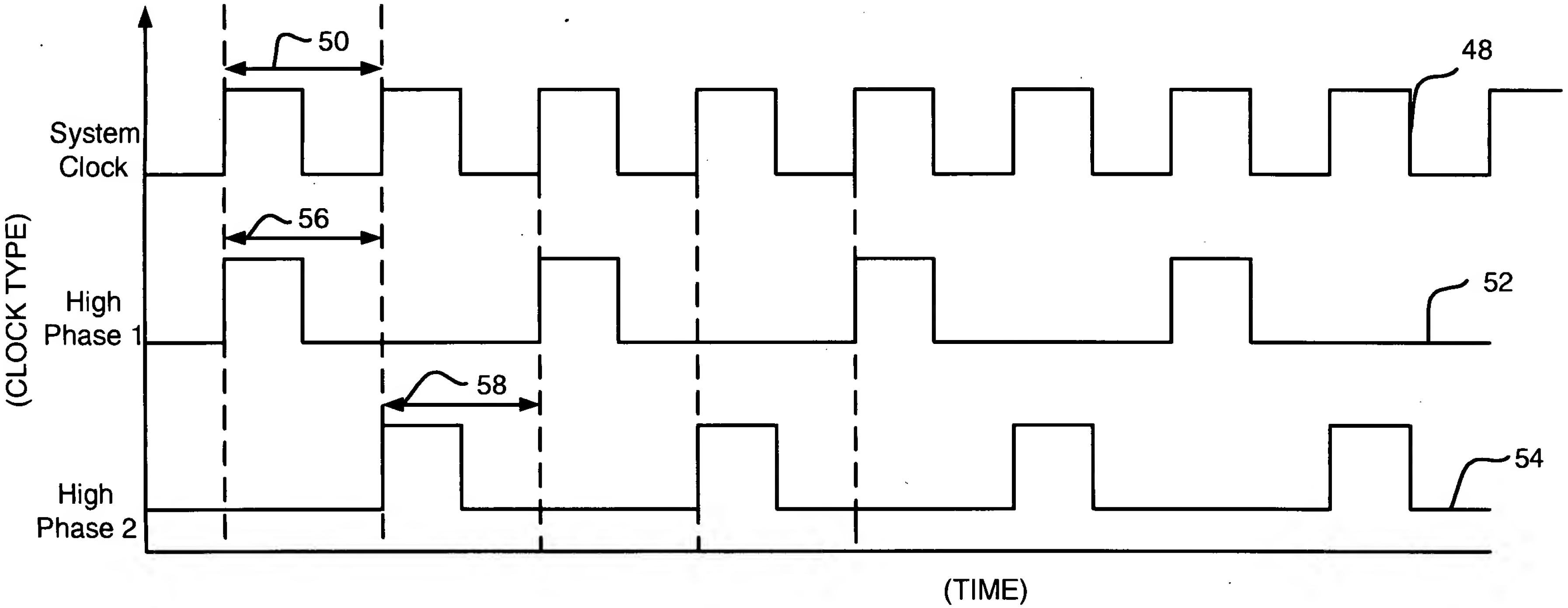
(CLOCK TYPE)
System Clock
High Phase 1
High Phase 2
(TIME)
50
56
58
48
52
54

FIG. 4

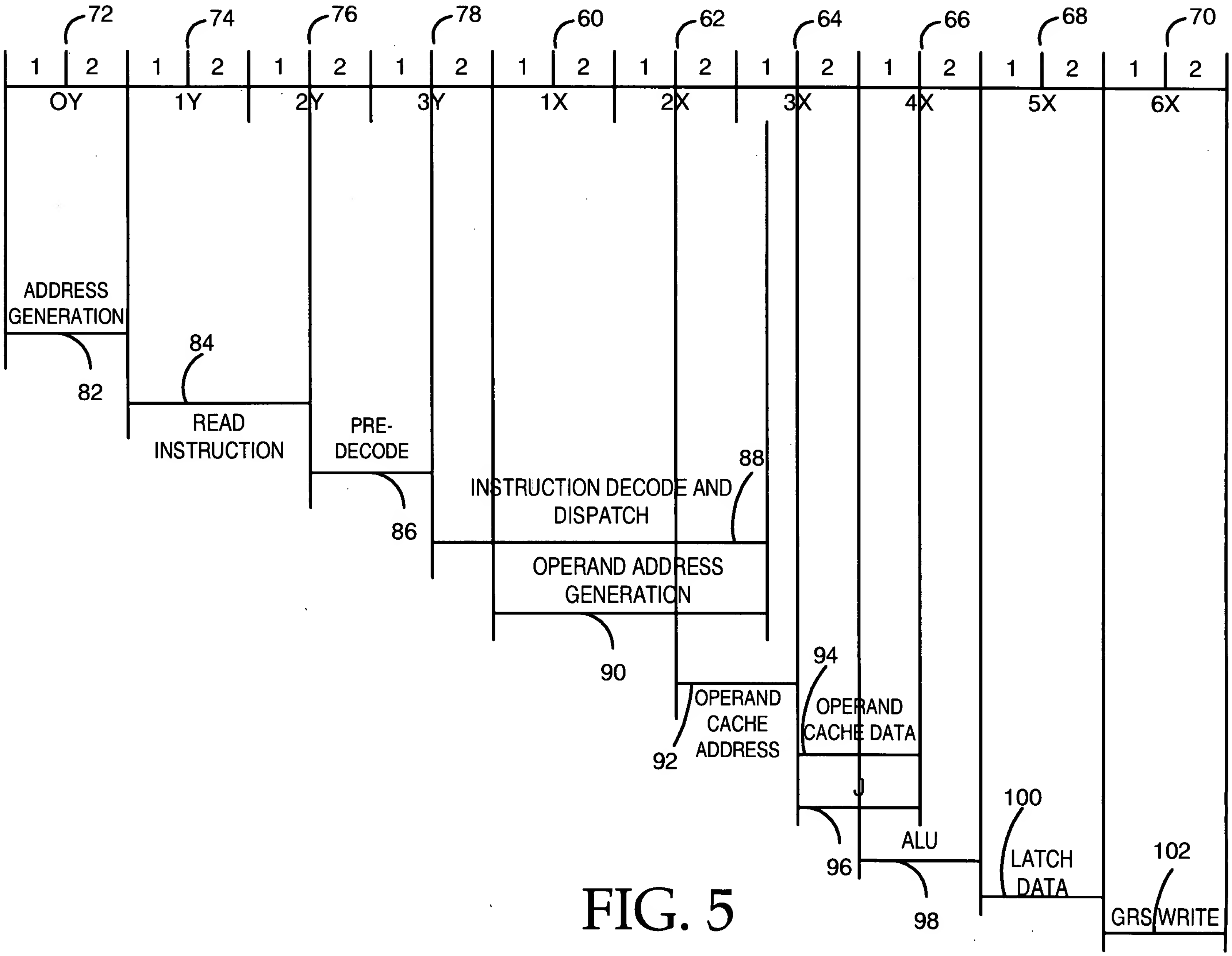
72
74
76
78
60
62
64
66
68
70
1
2
OY
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
ADDRESS GENERATION
82
84
READ INSTRUCTION
PRE-DECODE
86
88
INSTRUCTION DECODE AND DISPATCH
OPERAND ADDRESS GENERATION
90
94
OPERAND CACHE ADDRESS
92
OPERAND CACHE DATA
J
96
ALU
98
100
LATCH DATA
102
GRS WRITE

FIG. 5

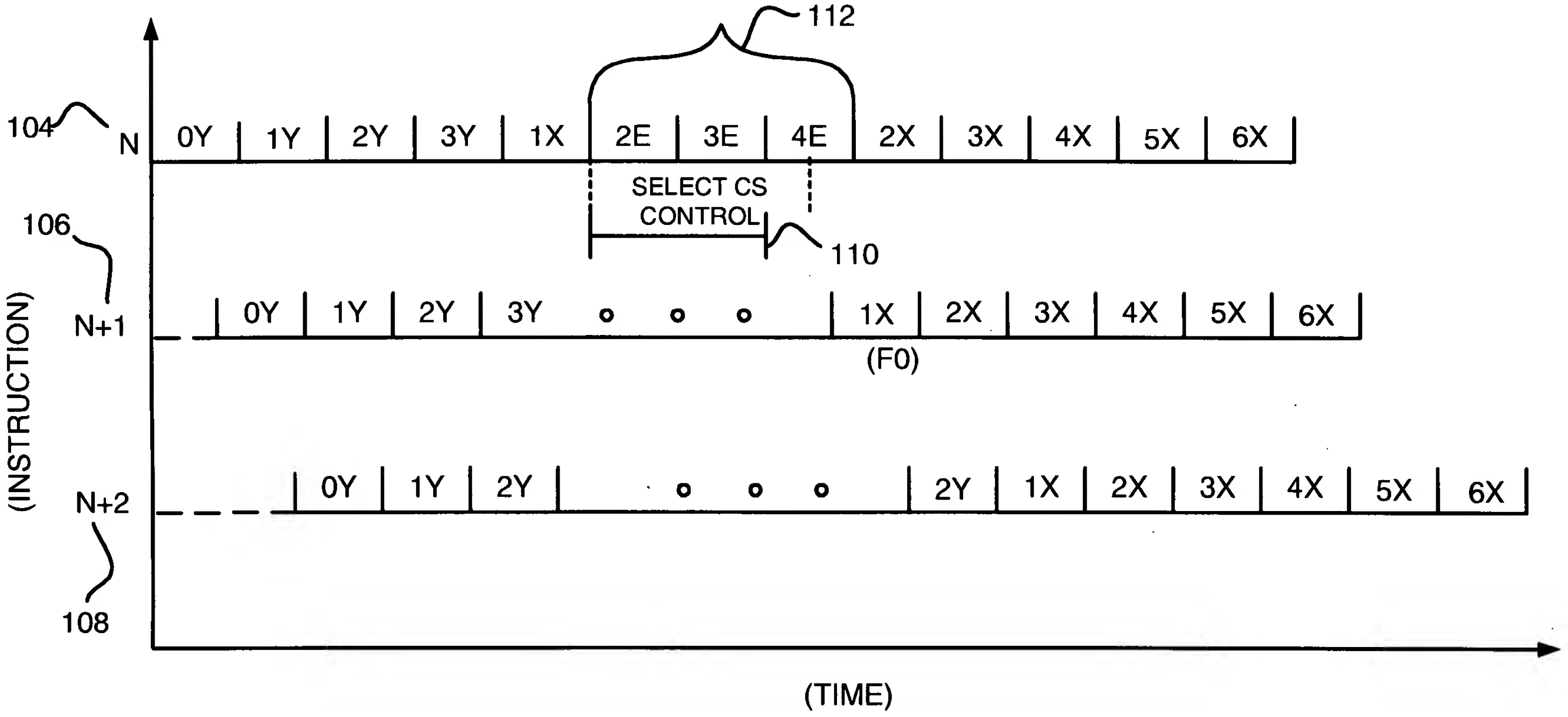
112
104
N
0Y
1Y
2Y
3Y
1X
2E
3E
4E
2X
3X
4X
5X
6X
SELECT CS CONTROL
110
106
N+1
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
(F0)
(INSTRUCTION)
N+2
0Y
1Y
2Y
2Y
1X
2X
3X
4X
5X
6X
108
(TIME)

FIG. 6

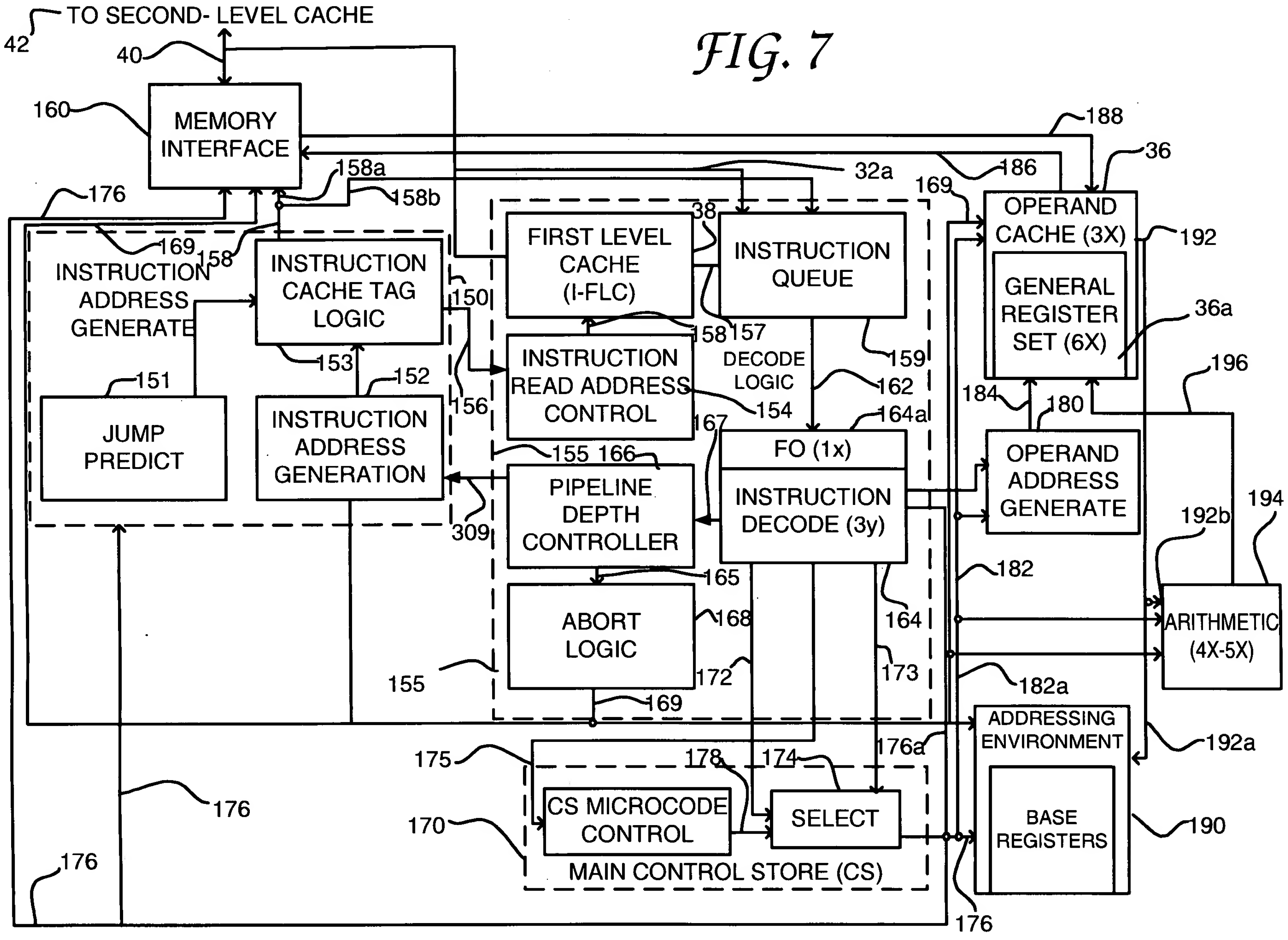

FIG. 7

42
TO SECOND- LEVEL CACHE
40
160
MEMORY INTERFACE
176
169
158
158a
158b
INSTRUCTION ADDRESS GENERATE
INSTRUCTION CACHE TAG LOGIC
153
150
151
JUMP PREDICT
152
INSTRUCTION ADDRESS GENERATION
156
309
32a
38
FIRST LEVEL CACHE (I-FLC)
INSTRUCTION QUEUE
158
157
159
INSTRUCTION READ ADDRESS CONTROL
DECODE LOGIC
162
154
164a
167
155
166
PIPELINE DEPTH CONTROLLER
FO (1x)
INSTRUCTION DECODE (3y)
165
ABORT LOGIC
168
164
155
172
173
169
175
178
174
176a
170
CS MICROCODE CONTROL
SELECT
MAIN CONTROL STORE (CS)
176
176
176
188
186
36
169
OPERAND CACHE (3X)
192
GENERAL REGISTER SET (6X)
36a
196
184
180
OPERAND ADDRESS GENERATE
182
194
192b
ARITHMETIC (4X-5X)
182a
ADDRESSING ENVIRONMENT
192a
BASE REGISTERS
190

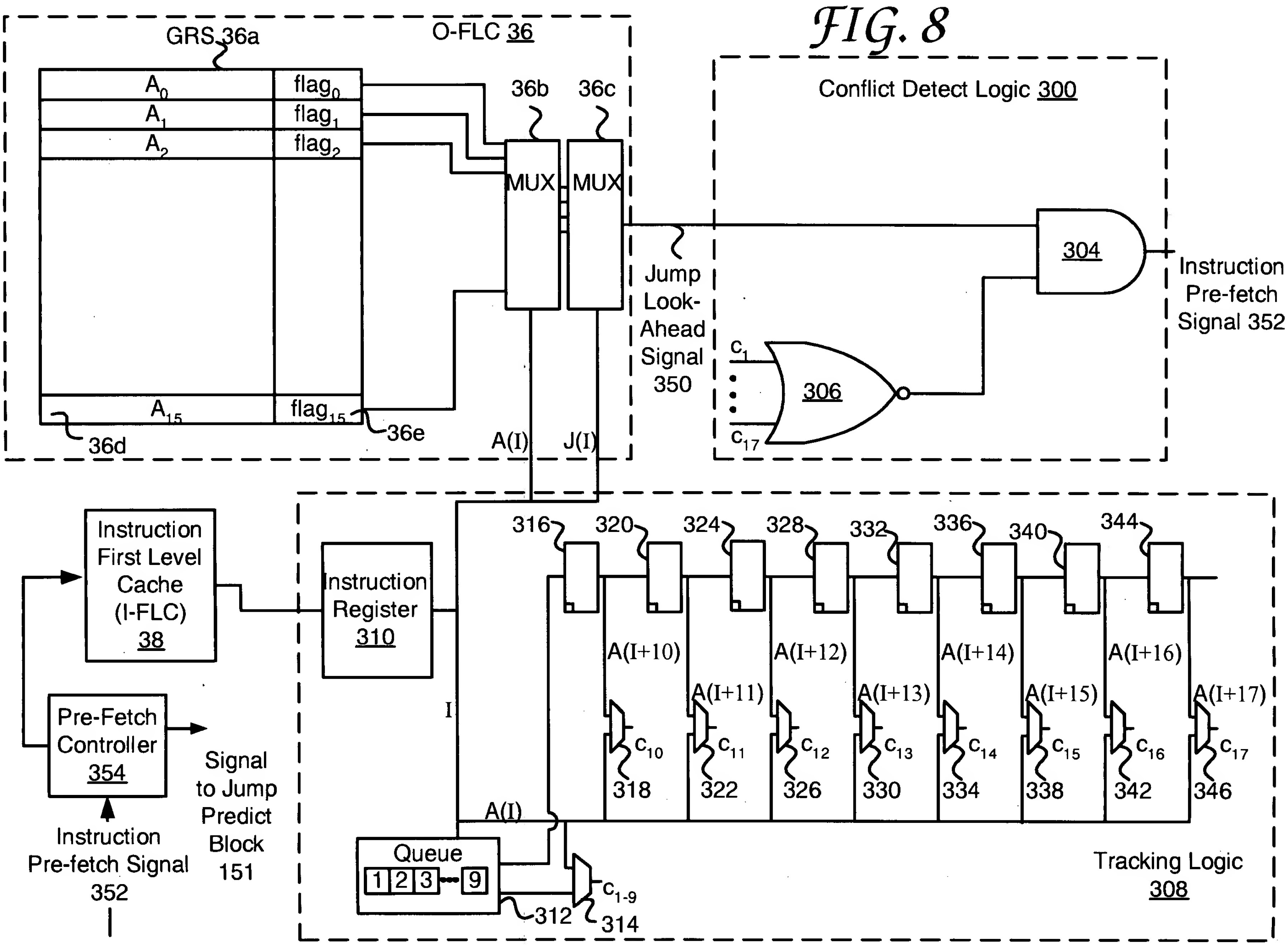
FIG. 8
O-FLC 36
GRS 36a
A0
A1
A2
A15
flag0
flag1
flag2
flag15
36d
36e
36b
36c
MUX
MUX
A(I)
J(I)
Jump Look-Ahead Signal 350
Conflict Detect Logic 300
304
306
c1
c17
Instruction Pre-fetch Signal 352
Instruction First Level Cache (I-FLC) 38
Instruction Register 310
I
Pre-Fetch Controller 354
Signal to Jump Predict Block 151
Instruction Pre-fetch Signal 352
316
320
324
328
332
336
340
344
A(I+10)
A(I+11)
A(I+12)
A(I+13)
A(I+14)
A(I+15)
A(I+16)
A(I+17)
c10
c11
c12
c13
c14
c15
c16
c17
318
322
326
330
334
338
342
346
A(I)
Queue
1
2
3
9
312
c1-9
314
Tracking Logic 308

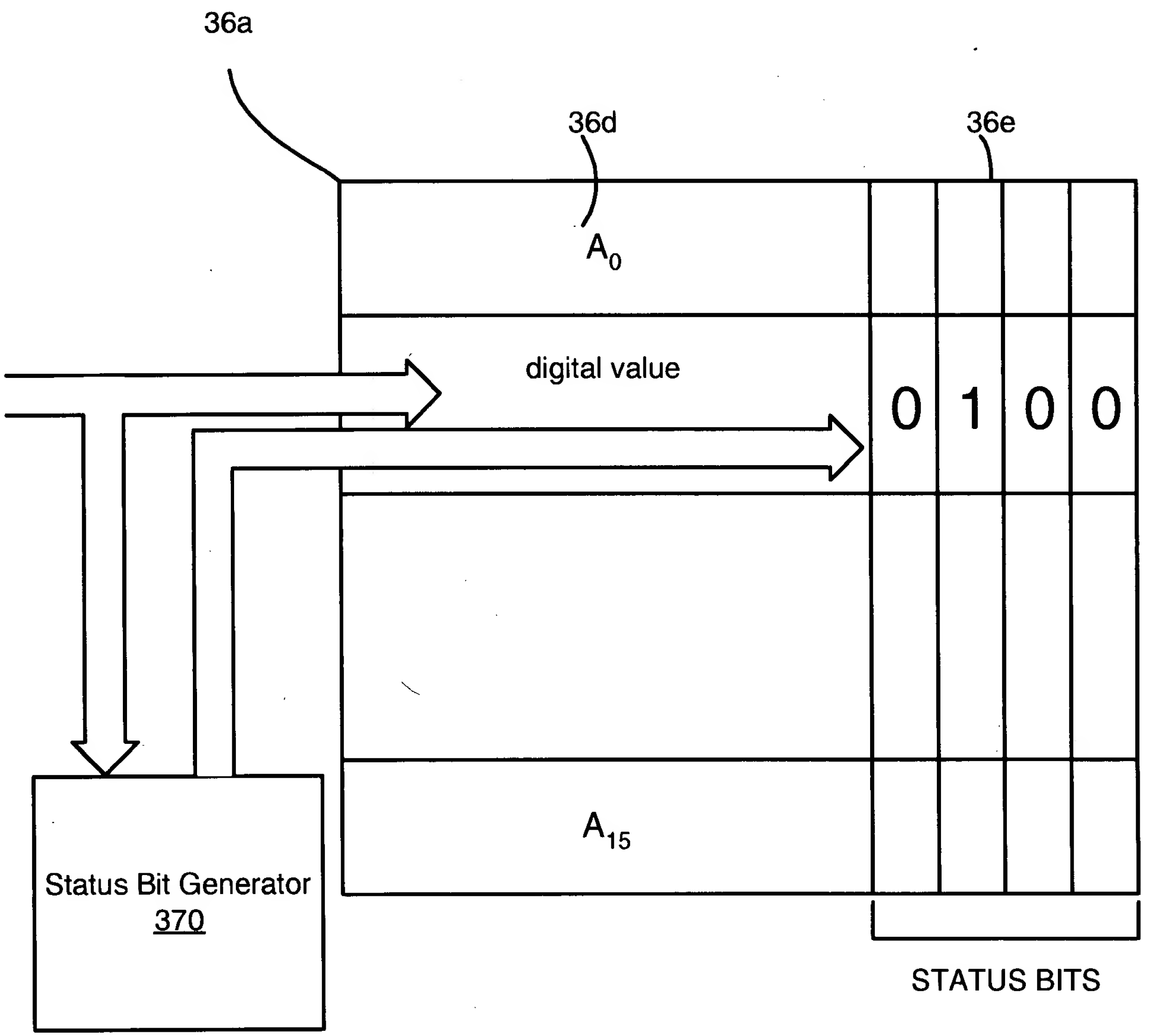
36a
36d
36e
A$_0$
digital value
0
1
0
0
A$_{15}$
STATUS BITS
Status Bit Generator
370

FIG. 9